



Part Number TL-152

[30-512] MHz Tunable Bandpass Filter

R3 June 2022

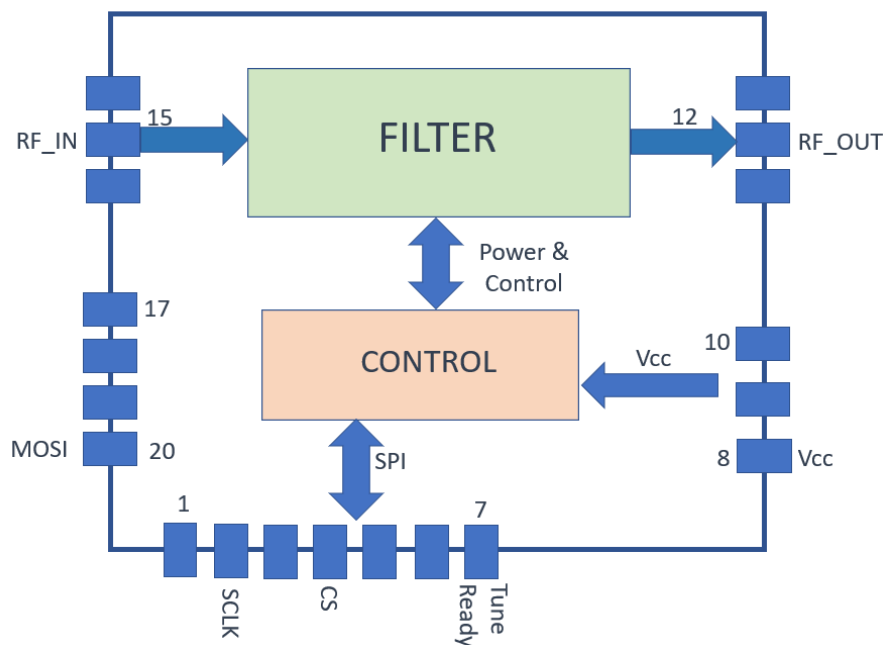
Features

- +24dBm Power Handling
- 120dBm Noise Floor
- Single +3.3V Supply
- Rejection @ 20dBc @ $f_c \pm 15\%$

Applications

- Full Tactical Communications bands
- Military Radar
- SATCOM
- Small Size, Medium Power Requirements.

Block Diagram





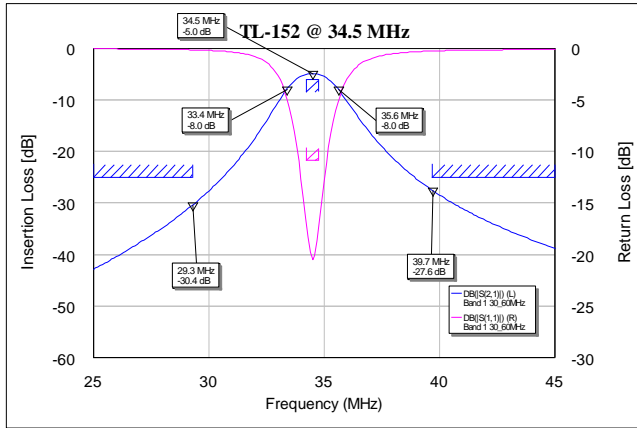
Specification

Parameter	Specification	Min	Typ.	Max	Units
Supply Voltage	-	+3.1	+3.3	+3.6	V
Supply Current	-	-	28	48	mA
Tunable Frequency Range	-	30	-	512	MHz
Input/Output Impedance	-	-	50	-	ohms
Return Loss	[30 – 512] MHz	9.54	13.98	-	dB
Insertion Loss	[30 – 512] MHz	-	6.0	7.0	dB
3dB Passband Bandwidth	[30 – 512] MHz	-	7.0	-	%
Rejection	Ftune +/- 15%	-	20	-	dBc
	30MHz to < 0.5*Ftune>	30	-	-	dBc
	[2*Ftune to 750] MHz	50	-	-	dBc
	[750 - 1000] MHz	30	-	-	dBc
P1dB	[30 - 512] MHz	24	-	-	dBm
IIP3	[30 - 512] MHz	36	-	-	dBm
Tuning Step Size	[30 - 90] MHz	-	0.25	-	MHz
	[90.5 - 219] MHz	-	0.50	-	MHz
	[220 - 512] MHz	-	1.00	-	MHz
Switching Speed	[30 - 512] MHz	-	25	35	µs
Noise Floor	[30 - 512] MHz	-	-120	-110	dBm
Operating Temperature		-40	-	+85	C
Settling Time	[30 - 512] MHz	-	-	20	µs

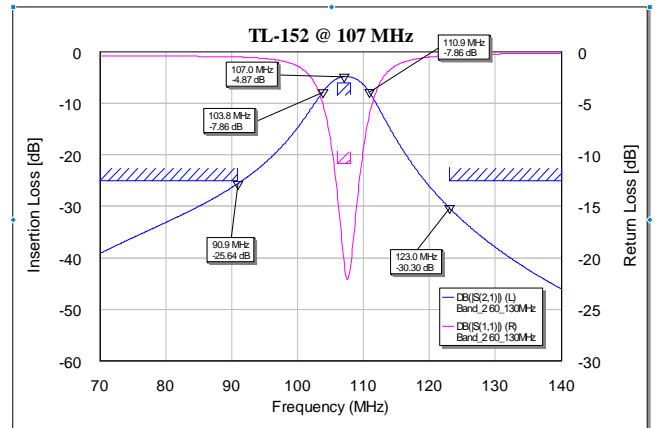
Environmental	Operating Temperature	[-40 to +85] C
	Vehicular Vibration	MIL-STD-810G, Method 514.6, Annex C, Category 20, and Category 4.
	Jet Fighter Vibration	MIL-STD-810F, Method 514.5, Annex C, Category 12.



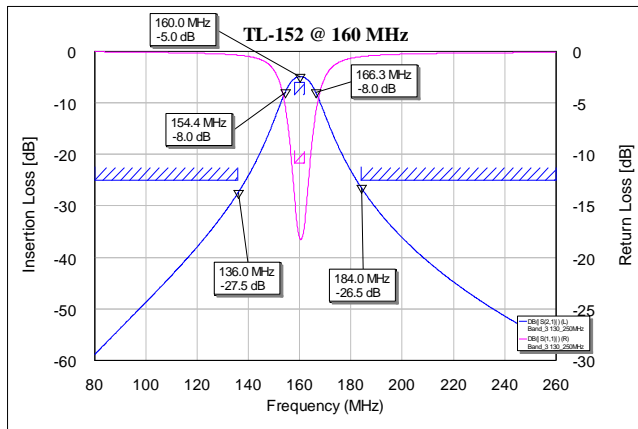
Modeled Data



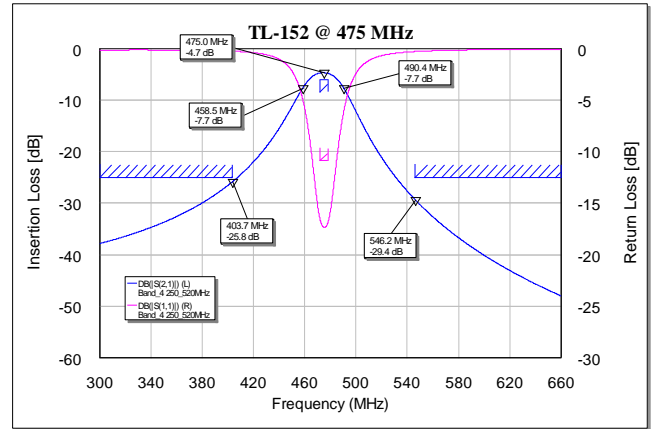
6.4% 3dB BW



6.6% 3dB BW



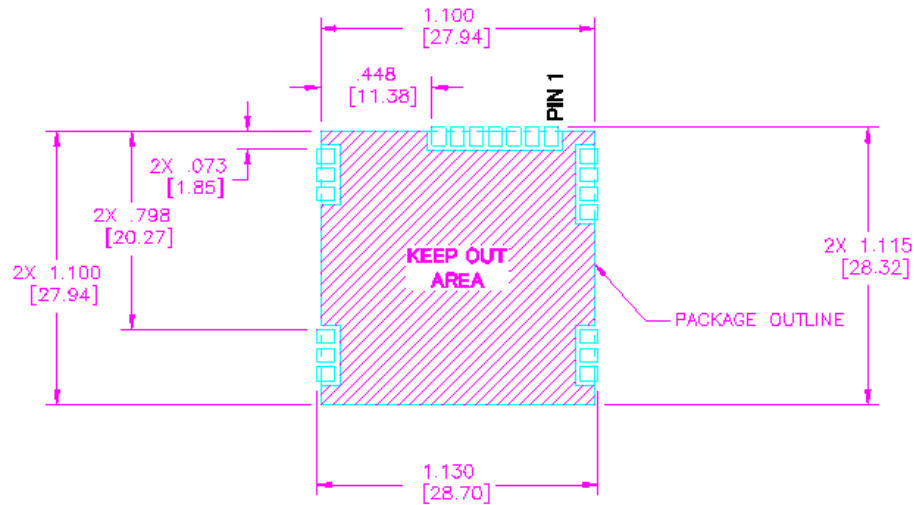
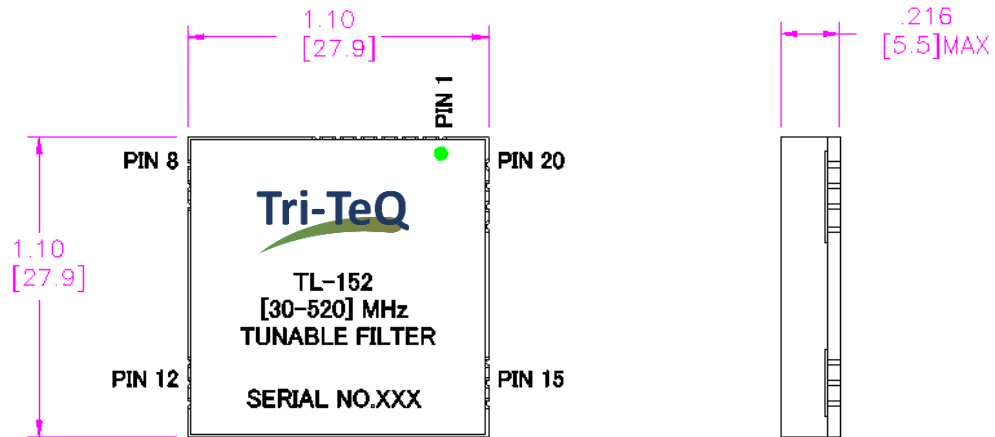
7.4% 3dB BW



6.7% 3dB BW



Outline Drawing



RECOMMENDED MOUNTING PATTERN

Pin Number	Label	Description
1, 3, 5, 6, 10, 18, 19	NC	No Connection. Factory Use Only
2	SCLK	Serial Tune Interface Clock
4	CS	Serial Chip Data Select
7	Tune Ready	Tune Ready Indicator
8	Vcc	Supply Voltage
9, 11, 13, 14, 16, 17	GND	Digital and Analogue Ground
12, 15	RF I/O	RF Input and RF Output Ports
20	MOSI	Serial Tune Interface Data Master Output Slave Input



TL-152 Control.

The TL-152 uses a SPI interface to input a 16-bit filter select word. The filter select word represents the 2 times target tune frequency in MHz. The tuning range is 30 to 520 MHz, so the valid filter select word range is 60 to 1040. The SPI interface is Write-only so there are only three SPI signals:

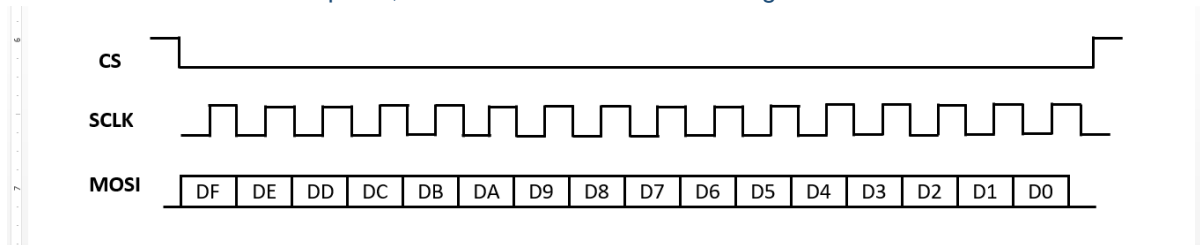
- CS: When CS is low, the SPI bus is enabled.
When CS is high, signals on the other SPI inputs are ignored.
- SCLK: Serial data clock generated by the SPI bus master.
- MOSI: Data from master to slave (Master Out, Slave In).
- MISO: Always Logic Low. [Internally factory set]

The timing of the SPI bus is:

- The base value of the clock is low (0).
- The unit reads the incoming data (MOSI) on the rising edge of the clock SCLK.
- The maximum allowed SCLK rate is 1.0 MHz

The figure below shows the SPI bus set command operation:

- The SPI bus master sets CS low and generates the SCLK.
- The master sends a 16-bit filter select word (MSB first) on the MOSI line.
- After the last clock pulse, the SPI bus master sets CS high.

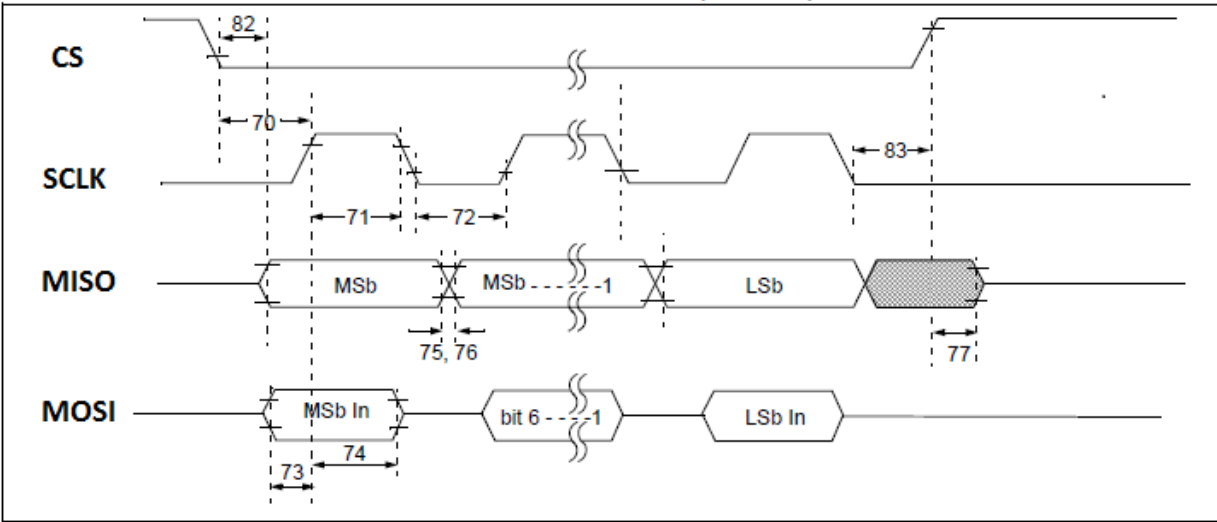


All Digital I/O are supplied at +3.3V.

- CS input: Logic low = 0.8V Max., Logic High = 2.0V Min.
- SCLK: Logic low = 0.2V Max., Logic High = 3.0V Min.
- MOSI: Logic low = 0.2V Max., Logic High = 3.0V Min.
- MISO: Output is always Logic Low = 0.8V Max



TL-152 SPI TIMING DETAILS



Param. No.	Symbol	Characteristic	Min	Max	Units
70	Tssl2sc	CS Fall or SCLK Fall or Rise	62.5	"	ns
71	Tsch	SCLK Input High Time	25	"	ns
72	Tscl	SCLK Input Low Time	30	"	ns
73	Tdi2sc	Setup Time of Data Input to SCLK Edge	25	"	ns
74	Tsc2di	Hold Time of Data Input to SCLK Edge	25	"	ns
75	TdoR	Data Output Rise Time	"	30	ns
76	TdoF	Data Output Fall Time	"	20	ns
77	TssH2Z	CS Rise to Data Output High Impedance	10	50	ns
82	Tss2doV	Data Output Valid After CS Falling Edge	"	60	ns
83	Tsc2ssH	CS Rise after SCLK edge	133.5	"	ns



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